Method for fabricating semiconductor memory device

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Abstract

A semiconductor memory device and fabricating method thereof including one transistor consisting of a source, a drain and a gate electrode, a bit line in contact with the drain region of the transistor via a first contact hole, a storage electrode in contact with the source region of the transistor via a second contact hole, a first planarized insulating layer formed under the bit line and a second planarized insulating layer formed under the storage electrode, whereby the material layer formed under the conductive layers, e.g., the bit line and storage electrode, is planarized to prevent stringers created due to surface indentations. Further, after a spacer is formed directly on the side walls of contact hole or on the side walls of a pattern for forming the contact hole, the contact hole is formed to prevent the contact between conductive layers, as a result, improving the memory device's reliability and being advantageous in realizing high density.